On-chip Parametric Test of R-2R Ladder Digital-to-Analog Converter and Its Efficiency

Daniel Arbet, Viera Stopjaková, Juraj Brenkuš, and Gábor Gyepes

***Abstract*—This paper deals with the investigation of the fault detection in separated parts of a mixed-signal integrated circuit example by implementing parametric test methods. The experimental Circuit Under Test (CUT) consisting of an 8-bit binary-weighted R-2R ladder digital-to-analog converter and additional on-chip test hardware was designed in a standard 0.35μm CMOS technology. For detection of catastrophic and parametric faults considered in different parts of the CUT, two dedicated parametric test methods: oscillation-based test technique and I_{DDQ} monitoring were used. For the operational amplifier, on-chip and off-chip approaches have been used to compare the efficiency of both approaches in covering catastrophic faults that are hard to detect. For respective converter parts, the excelent fault coverage of 94.21% of hard-detectable faults by the proposed parametric tests was achieved.**

***Index Terms*—Fault detection, catastrophic faults, parametric faults, on-chip parametric test, mixed-signal test**

I. Introduction

THE present trends in the development of integrated circuits and new advanced technologies enable integration of complex digital and mixed-signal systems on a single chip. These complex systems, know as Systems-on-Chip (SoC), can include digital, analog, and RF circuits as well as MEMS structures, microsensors and another different cores. No doubt, testability of the respective parts in such systems is greatly decreased [1]. Standard test methods cannot be straightforwardly used to test complex mixed-signal systems. Therefore, several automatic test equipments (ATE), each dedicated to a particular core integrated in the system, would be needed. Such approach increases costs of IC production unacceptably, since it requires the expensive and advanced ATE. Due to this reason, test methodology for complex systems becomes the upmost important. Test engineers have been looking for new test methods and approaches, which can assure better testability, higher fault coverage and high quality of integrated system production.

Parametric test methods are most commonly used for testing analog and mixed-signal integrated circuits (IC). These methods are based on the monitoring of a specific circuit's parameter such as voltage, supply current, frequency, etc. Evaluation of the specific parameter in a complex system is difficult because it requires sophisticated sensing and analyses of the selected parameter in terms of additional hardware needed, setting the Pass/Fail limit, robustness, etc. (in comparison to the simple logic test). On the other hand, parametric test, performed for a part of the complex system, may be the only proper and/or implementable test approach in some applications [2]. Such approach is based on dividing the complex system into smaller parts that could be easily tested separately, each part by a dedicated test method.

In this paper, an 8-bit R-2R ladder digital-to-analog converter (DAC) was used as the test vehicle. Considering the structure of this circuit, it was split into two parts, which have been tested separately using two different parametric test methods. Thus, the control logic, used for selecting the test method and switching the circuit mode (test/functional), has been designed. In Section 2, the preliminary work done in the respective area is described. Experimental CUT is presented in more details in Section 3. In Section 4, the proposed test strategies employed in test of the respective part of the DAC are described. In Section 5, influence of additional test hardware on the DAC preformance is addressed. Simulation results and achieved fault coverage are summarized in Section 6. In the last section, the efficiency of the proposed test method through the obtained experimental results is discussed.

II. Preliminary Work

Digital-to-analog converters and analog-to-digital converters (ADC) are very often used circuits in the mixed-signal integrated systems. However, to test such systems by conventional external approaches, accurate measurement instruments as well as advanced and costly ATE [3] are necessary. Therefore, Built-In Self Test (BIST) approaches represent the best solution or sometimes, even the only possible way of testing mixed-signal circuits like converters are. Thus, BIST can significantly reduce test time and overall cost since the most difficult tasks are performed directly on a chip.

In the last years, many BIST structures have been published, and several different modifications of BIST approach applicable to DAC and ADC have been proposed [4]–[6]. The IEEE standard for terminology and test methods of digital-to-analog converters is described in [7]. In [8]–[10], different on-chip test hardware has been proposed and used for testing the data converters. BIST metodologies using different on-chip input stimuli generators were described in [11] and [12]. A BIST scheme for DAC testing, based on the under-sampling technique presented in [13], was proposed in [14]. The oscillation-based test for analog-to-digital and digital-to-analog converters has been addressed in [6], [15] and [16].

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Another BIST structures for very popular R-2R ladder DAC were addressed in [9], [17].

However, the efficiency of the existing on-chip test approaches in covering real hard-detactable faults has still some limitations, and it shoud be improved in order to assure the necessary reliability. Moreover, most of the parametric test methods are not mature enough to be implemented as fully on-chip test approach, since they suffer either from complexity of the hardware or from test stimuli gereration.

In this paper, on-chip parametric test of 8-bit R-2R ladder DAC is presented. The converter is split into two parts: the operational amplifier and R-2R resistor network, which are tested separately by oscillation test method [18]–[21] and I_{DDQ} monitoring [22]–[25], respectively. This approach is easy to implement and offers rather high fault coverage of hard-detectable faults. Furthermore, input test stimuli are easy to generate on-chip, and the proposed approach is able to identify a defective part of the CUT.

III. Experimental Circuit Under Test

Fig. 1 shows the block diagram of the experimental mixed-signal circuit designed in 0.35μm CMOS technology, which consists of the selected converter and the necessary on-chip test hardware, including the control logic used for switching the circuit into the test mode. As a mixed-signal CUT, an 8-bit binary-weighted R-2R ladder DAC have been designed and used in our experiment. In the test mode, the DAC circuit is split into two separated parts: a 2-stage operational amplifier (OPAMP) and the R-2R resistor network. Using two additional inputs TEST and MODE, the circuit can be switched in one of two test modes in order to test the respective part of the converter separately, each by employing a dedicated parametric test method.

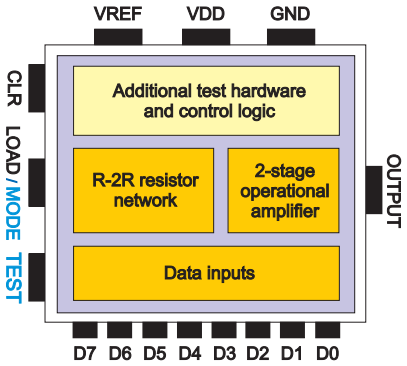

Fig. 1. Block diagram of the mixed-signal CUT used

IV. Proposed Test Strategy

A. Off-chip test of operational amplifier

For the fault detection in the operational amplifier (OPAMP), the oscillation test method transforming the amplifier into an oscillator by inserting a feedback RC network was used. Using this method, different faults present in the amplifier and causing deviation either in the oscillation frequency or in the amplitude of oscillations (exceeding the nominal fault-free tolerance range) can be detected [20].

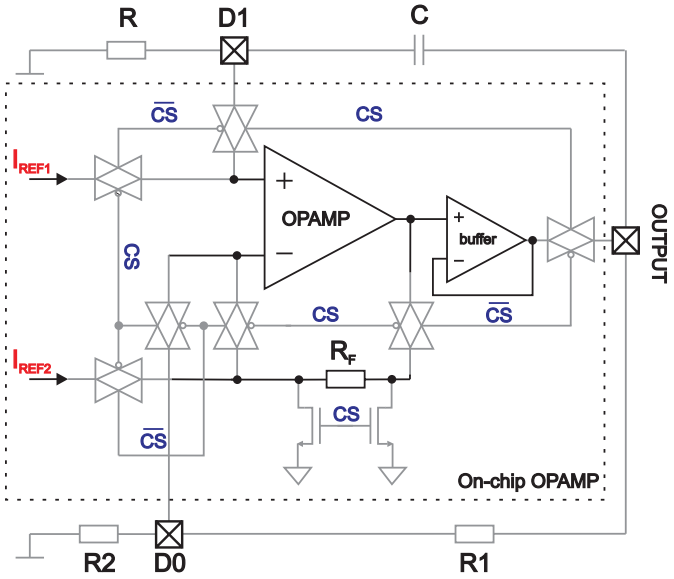

Fig. 2. Circuit diagram of the OPAMP circuit transformed into an oscillator (without control logic)

Components in the feedback network were connected externally (by T-gates) using two additional input pins (DO and D1) and the output pin OUTPUT (Fig. 2). In this configuration, a smaller deviation in the oscillation frequency and the amplitude of oscillations were reached. The feedback resistor R_F, which is a part of the DAC, is clamped to ground using two MOS transistors. A buffer is a default part of the converter but in this topology, it was also used to separate the OPAMP from possible external influences. The OPAMP can be tested by applying logic 1 and logic 0 to pins TEST and MODE, respectively (Fig. 1). Then the common control logic (not depicted in Fig. 2) generates the control signals (CS) for T-gates that for test purposes, disconnect the OPAMP from the R-2R resistor network and connect the feedback network.

T-gates were used for insertion of the feedback. However, they may cause the CUT performance degradation and therefore, their ON- and OFF- resistances must be as low as possible and as high as possible, respectively. Hence, the ON-resistance of T-gates, which are appearing in the signal path, must be minimized to prevent the undesired performance degradation [26].

The fault-free tolerance bands (representing process variations and temperature influence) for the oscillation frequency and the amplitude of the oscillation frequency were obtained by Monte Carlo analysis, and are depicted in Fig. 3 and Fig. 4, respectively. Deviations (obtained by 50 runs) of $\pm 13\%$ in the oscillation frequency and of $\pm 2.85\%$ in the oscillation amplitude were observed.

B. On-chip test of operational amplifier

Previously, the feedback network and passive components were realized externally using discrete devices in order to achieve higher accuracy and smaller deviation in the oscillation

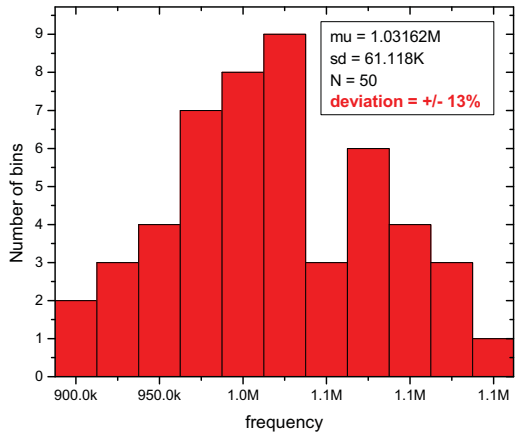

Fig. 3. Nominal deviation in the oscillation frequency

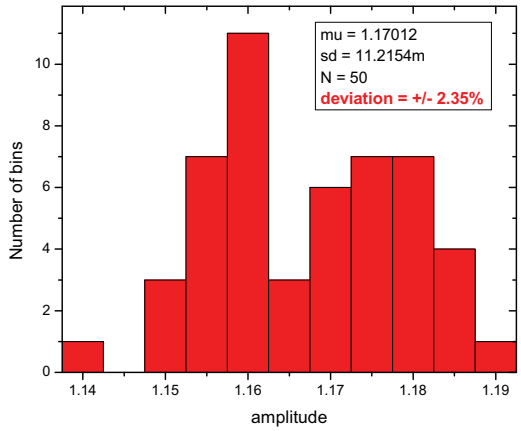

Fig. 4. Fault-free deviation in the amplitude of oscillations

frequency and the amplitude of oscillations. Taking into account SoC testing requirements, where a sort of BIST strategy to test the mixed-signal cores (e.g. DACs) is demanded, an on-chip test should be performed. Therefore, in such case, the OPAMP feedback network must be connected internally, using devices with about 20% deviation in technology parameters. In [21], such OBIST strategy for testing OPAMP as a part of complex analog and mixed-signal systems is described. To evaluate the efficiency of this test strategy, the circuit oscillation frequency is then compared to the reference frequency given by a Schmitt trigger oscillator, which was used as the on-chip frequence reference to compensate technology variations. Fig. 5 shows the circuit diagram of the on-chip oscillator using an on-chip feedback network for transforming the OPAMP into the oscillator.

The oscillation frequency was evaluated by countering a number of oscillation pulses exhibited by the CUT during a time interval generated by the reference oscillator. Influence of technology variations on the oscillation frequency for fault-free CUT was obtained from Monte Carlo analysis. MC analysis of technology variations of $\pm 3\sigma$ was performed for all devices used in the CUT and additional test hardware. To demonstrate the efficiency of the on-chip oscillation test approach, the fault-free tolerance bands obtained for the on-chip feedback network realization was compared to the one

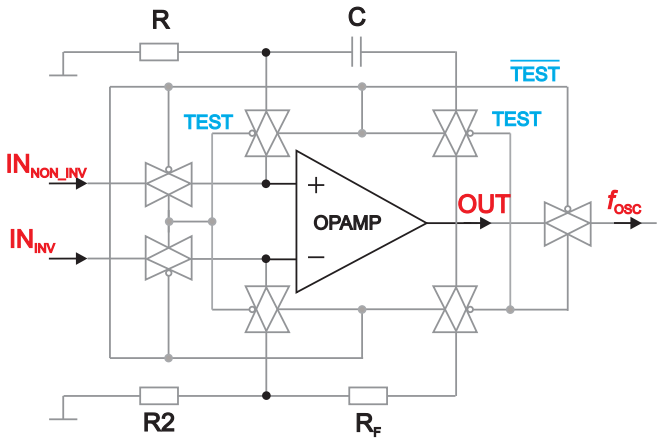

Fig. 5. Circuit diagram of the OPAMP circuit transformed into an oscillator (without control logic)

obtained for external reference oscillator (Fig. 6).

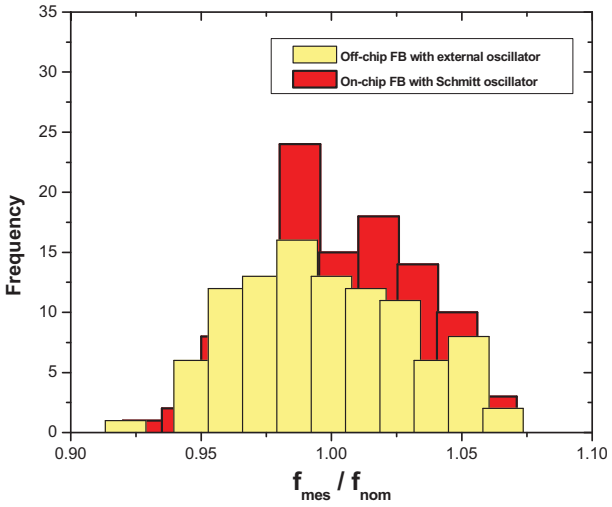

Fig. 6. Comparison of the oscillation frequency tolerance bands for on-chip and off-chip reference oscillator solutions

From Fig. 6, one can observe that deviation in the oscillation frequency for the on-chip feedback network and the on-chip reference oscillator is pretty much the same as the oscillation frequency deviation obtained by off-chip feedback network and the external oscillator. This result proves that the oscillation test strategy offers the on-chip test of the operational amplifier as a separated part of the experimental DAC. With the on-chip test, standard mixed-signal SoC test requirements could be fulfilled. A more detailed description of the proposed on-chip test strategy, including the oscillation frequency evaluation and the PASS/FAIL threshold selection, is presented in [21].

C. Test of R-2R resistor network

The R-2R ladder is a resistor network that uses a cascaded structure of current dividers, which generate binary-weighted currents in the respective branches, as shown in Fig. 7. In ideal

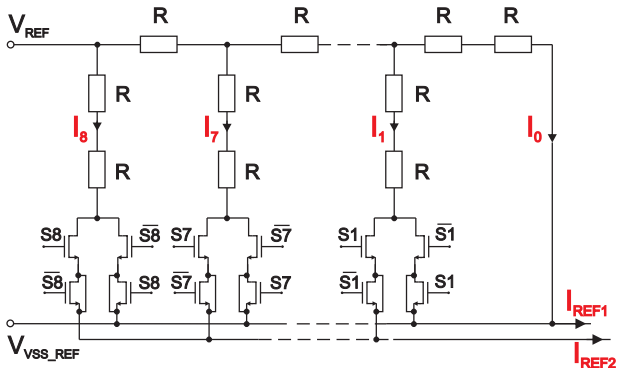

Fig. 7. Circuit diagram of the R-2R ladder

case, the dividing ratio should be 2:1 but because of resistors mismatch, in reality, the divisions will be imperfect.

The most probable fault in the resistor ladder is that the value of a resistor exceeds its tolerance band (parametric fault). These faults can be detected by the measurement and evaluation of current value in the respective current branches. The described technique has been used for parametric test of the R-2R ladder, which represent a substantial part of the whole DAC circuit. Modification of this method, used in digital IC test, is known as I_{DDQ} testing.

Principle of current testing of the R-2R ladder is as follows: in the first step, current I8 is compared to the sum of currents I7 to I0, then in the second step, the control logic turns-off switches S8 and $\overline{S8}$, and current I7 is compared to the sum of currents I6 to I0. Consequently, control logic turns-off switches S7 and $\overline{S7}$, and another two currents are compared. This procedure goes on till the last two current branches are processed.

The current difference at each step of the proposed test procedure can be expressed as follows:

$$I_{diff\_N} = I_N - \left(\sum_{i=0}^{N} I_{N-1}\right) \tag{1}$$

where N = 1, 2, 3, ... 8 and IN is current in the respective branch being sensed.

Circuit diagram of R-2R ladder with the additional test hardware is depicted in Fig. 8. In every branch of the resistive network, two T-gates were included to switch-off the corresponding branch. Control signals for T-gates (CS, $\overline{CS}$ and also CS_1 - CS_8) were generated by the common control logic. Circuitry performing the current difference consists of three cascode current mirrors, as shown in Fig. 8 (right side). This circuit also ensures that the differential current (difference of I_{REF1} and I_{REF2}) will flow out to the circuit's output.

This approach can test the resistor ladder in total eight steps, by shifting the logic 1 from MBS to LSB. The main problem of this method is that current in the last branch is in order of nA, which is difficult to sense and measure with necessary precision. Therefore, this test technique might be limited to ladders that use resistors with the resistance value smaller than 10kΩ. A fault-free tolerance band of the differential current I_{diff} was obtained by Monte Carlo analysis and achieved results will be presented in the following section.

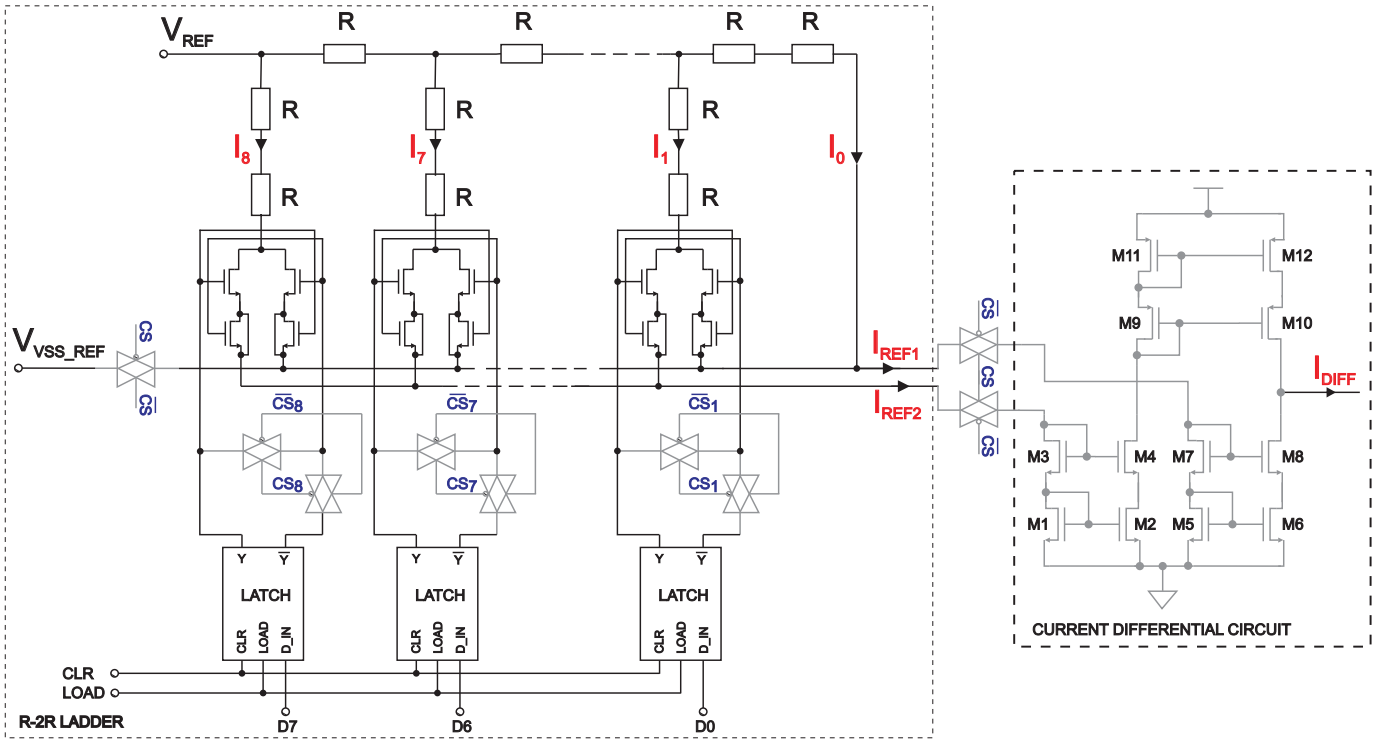

Fig. 8. Circuit diagram of R-2R ladder with additional test hardware (without control logic)

V. Influence of Additional Test Hardware

Insertion of the necessary on-chip test hardware might undesirably affect the DAC performance. The main reason is probably the use of T-gates (disconnecting the individual parts), which have some resistance in switch-on state. The most critical are T-gates that are connected in the path leading to the circuit output. Fig. 9 shows how the integral and the differential nonlinearity (INL' and DNL') of the DAC (with the test hardware) depend on the ON resistance of T-gates connected in the path leading to the converter output.

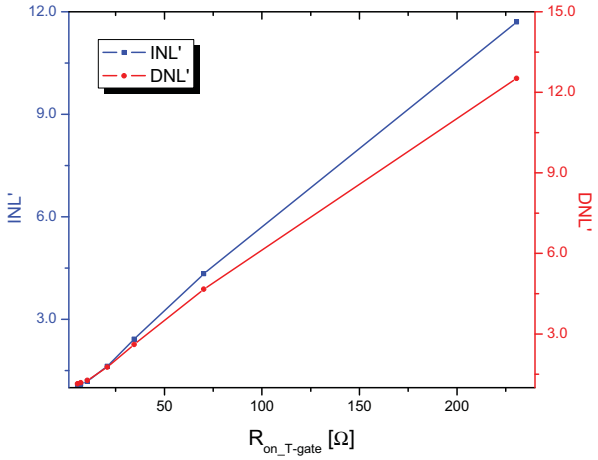

Fig. 9. INL' and DNL' versus R_{ON} of T-gate

It can be observed that in order to maintain the original parameters of DAC, R_{ON} of T-gates should be order of tens of Ohms. If the T-gates with R_{ON} of about 10 Ω are used, the value of integral and differential nonlinearity will be increased by 18% and 27%, respectively. In such case, the additional test hardware will require the area of 0.002 mm^2, which means that the total area will be enlarged by 13%. From the aspect of testing it is therefore, necessary to find a good compromise between the CUT performance and the test hardware area overhead.

Fig. 10 and Fig. 11 show how the other main parameters of the digital-to-analog converter (with the additional test hardware) depend on the switch-on resistance of T-gates connected in path leading to the converter output.

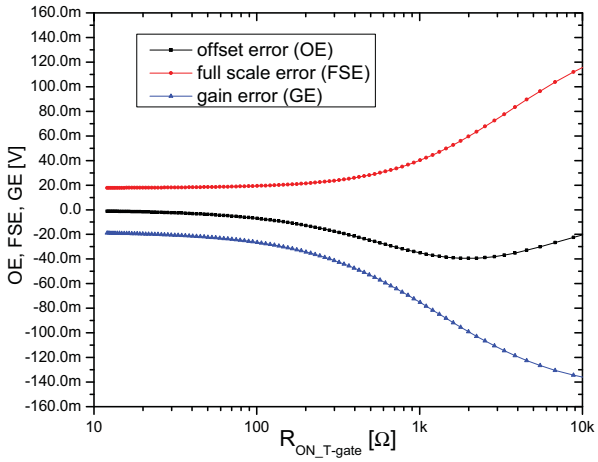

Fig. 10. OE, FSE and GE versus R_{ON} of T-gate

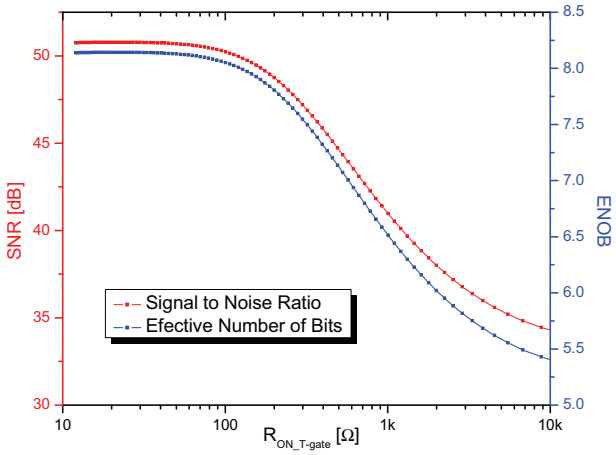

Fig. 11. SNR and ENOB versus R_{ON} of T-gate

It can be observed that to maintain the original value of the full scale error (FSE), signal-to-noise ration (SNR) and effective number of bits (ENOB) parameters, it would be sufficient to use T-gate with R_{ON} of about 100 Ω. However, achieve the original values of INL, DNL, offset error (OE) and gain error (GE), R_{ON} should be about of tens of Ohms. Thus, it can be concluded that to maintain the original value of all parameters of the converter, R_{ON} of T-gates should be kept in the range from 10 to 100 Ohms. In this case, the total area overhead would be enlarged from 6.5% to 13%.

VI. Achieved Results

For verification of the efficiency of the proposed test methods in testing parts of DACs, four types of catastrophic faults in the OPAMP, and two parametric faults in the R-2R ladder were considered. Catastrophic faults such as shorts, opens, gate-oxide shorts (GOS) and floating gates (FG) were inserted. Short and open faults were injected in all connection paths, while GOS and FG faults were applied in all transistors forming the OPAMP. Parametric faults, which most commonly arise on passive devices, were modeled and injected in the R-2R resistor network.

A. Results of the operational amplifier test

In the operational amplifier, several catastrophic faults such as opens and shorts as well as floating gates and gate-oxide-shorts, were considered. For their detection, the oscillation-based test method of the OPAMP circuit was employed.

Opens were modeled using a parallel combination of a resistor and a capacitor. Resistors and capacitors values depend on the defect location and size. We have considered nine different open faults injected in 24 different locations. From all considered 216 opens, 209 faults were detected, which means that the fault coverage of 94% was achieved. However, opens modeled with the resistance value of 1 MΩ represent so call *hard-detectable* faults. Thus, opens having higher resistance would probably not be covered by other test technique either.

Short faults were modeled and simulated using a serial short resistor. Values of resistors considered as short faults are as follows: 500 Ω, 1k Ω, 10k Ω, 100 kΩ and 1 MΩ. The achieved fault coverage, presented for different ranges of the short resistance value, is presented in Table I.

TABLE I
FAULT COVERAGE OF SHORT FAULTS

$\mathbf{R_{short}}$ [Ω]	500 ÷ 10k	500 ÷ 100k	500 ÷ 1M
Fault Coverage	100%	95.58%	84.7%

It can be observed that shorts with lower resistance are easier to detect because, in most cases, such shorts lead to loss of the oscillations or significant deviation in the amplitude of oscillations. Shorts with the resistance higher than 100 kΩ usually cause only slight deviation in the oscillation frequency that makes them more difficult to detect.

For floating gates (FG) we used an extended electrical model described in [27], considering also capacity of the break. Hence, the FG fault model includes capacitors C_{mp}, C_{pb} and C_{break}, which values were set to 2.82 fF, 3.02 fF and 0.07 fF, respectively. All considered FG faults were easily detected through either loss of the oscillation or a change in the oscillation frequency (single fault). The worst case of the overall fault coverage of all catastrophic faults, using the external oscillator feedback network, is summarized in Table II.

TABLE II
WORST CASE OF OFF-CHIP TOTAL FAULT COVERAGE

Faults	**Fault coverage**
Shorts	84.7%
Opens	94%
FGs	100%
Total	**92.9%**

The total fault coverage achieved for on-chip realization of the proposed parametric test of the OPAMP block is summarized in Table III.

TABLE III
TOTAL FAULT COVERAGE FOR ON-CHIP TEST OF OPAMP

Faults	**inserted**	**detected**	**Fault coverage**
Shorts	68	54	79.41%
Opens	216	180	83.33%
FGs	9	7	77.77%
Total	**293**	**241**	**82.25%**

The off-chip approach offers slightly higher total fault coverage than the one achieved in case of on-chip test realization. On the other hand, on-chip approach enables a BIST that is typical for SoC testing. However, some of the undetected faults have been manifested by a certain deviation in the amplitude of oscillations (not evaluated in our experiment). Therefore, the total fault coverage might be increased further by evaluation of this parameter. The obtained results prove that the oscillation-based test approach can be relatively very efficient in detecting different catastrophic faults (including hard-detectable ones) in analog sub-circuits.

We also analyzed the possible dependence of the fault coverage in the OPAMP on the value of the oscillation frequency. To test the amplifier by oscillation-based strategy at different oscillation frequencies, the value of passive devices used in the positive feedback loop was varied. The fault coverage dependence on the value of the oscillation frequency for different shorts and floating gates is shown in Fig. 12 and Fig. 13, respectively.

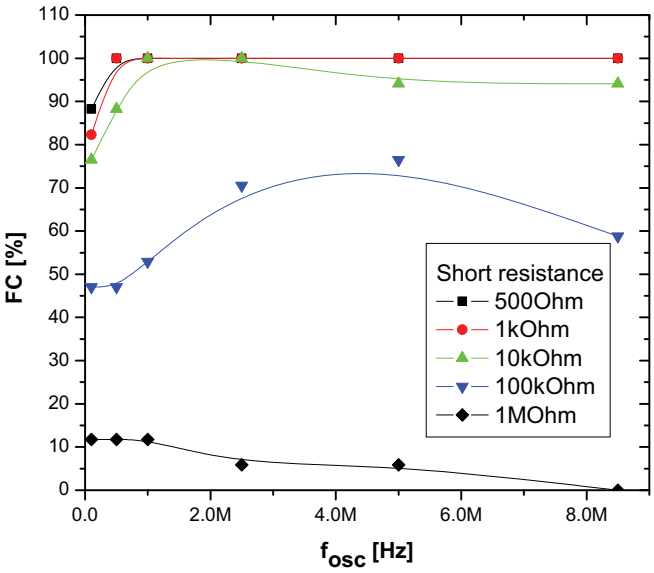

Fig. 12. Fault coverage versus the value of the oscillation frequency for different shorts

One can observe that the best fault coverage can be achieved at the oscillation frequency of about 2 MHz. Shorts with lower resistance are easy to detect since they usually cause loss of oscillations. Shorts with higher resistance (e.g. of 100 kΩ, 1 MΩ) cause deviation from the oscillating frequency, which

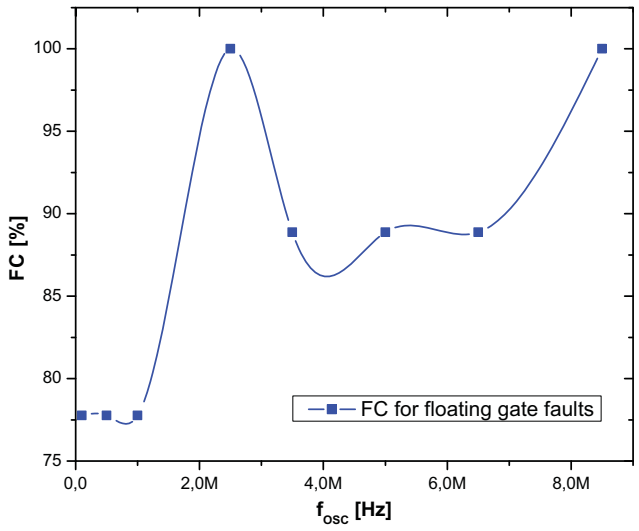

Fig. 13. Fault coverage versus the oscillation frequency value for floating gate faults

makes them more difficult to detect. Generally, the shorts with lower short resistance are easily detectable at lower oscillation frequencies, while the shorts with higher resistance (in order of 100 kΩ) are better covered at the higher frequency (about 4.5 MHz). Finally, shorts with resistance of 1 MΩ have lowest fault coverage in whole frequency range but those faults have a low probability of presence.

Secondly, the fault coverage dependence on the value of the oscillation frequency for floating gate faults was investigated (Fig. 13). It can be observed that 100% fault coverage can be achieved for the value of the oscillation frequency of 3 MHz and also for values higher than 8 MHz. Unfortunately, for the frequency higher than 8.5 MHz the CUT does not fulfill the conditions needed for the appearance of sustained oscillations.

B. Results of R-2R ladder test

In contrast to the OPAMP test, parametric faults were considered in the resistor network (R-2R ladder), and the fault coverage by the proposed current test method was investigated. Possible parametric faults in the resistor network were simulated using a resistor with varying its resistance value. It was considered that the value deviates by 5% or 10% from the tolerance range. Fig. 14 shows the tolerance band and simulated values of the output differential current depending on the test vector being applied.

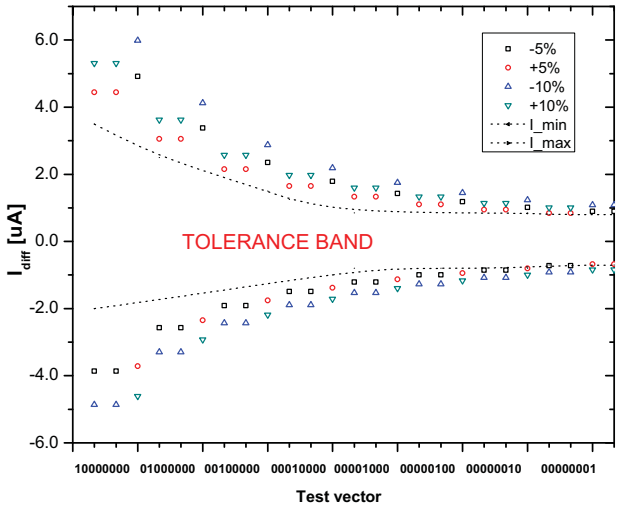

Fig. 14. Tolerance band and simulated values of the differential current in R-2R ladder

The simulation results show that almost all parametric faults in the resistor network are detectable. However, parametric fault considered in the last branch is difficult to detect because the current is too small to be sensed precisely. Table IV shows the fault coverage achieved by current monitoring approach for parametric faults considered in the resistor network. It can be observed that 10% deviation in resistors value is fully detectable and 100% fault coverage is reached. When the resistors value deviates from its tolerance band by 5%, the fault coverage is slightly lowered to 96% that is still very good result.

Finally, we can state that the proposed current test method is easy to implement and provides very high efficiency in covering parametric faults. However, the method might be limited by resistance values of resistors used in the ladder, since high values lead to less current flowing through the respective branches, which is rather difficult to be measured and processed.

TABLE IV
FAULT COVERAGE OF SHORT FAULTS

Parametric fault	±5% deviation	±10% deviation
Fault Coverage	96%	100%

VII. DISCUSSION & CONCLUSION

Two different parametric test methods have been used for on-chip fault detection in the R-2R ladder digital-to-analog converter. For this purpose, an experimental circuit, consisting of the DAC, the additional test hardware, and the control logic for switching the DAC between functional and test modes, has been designed in selected CMOS technology. The control logic was used to split the circuit into two parts, each tested separately by a dedicated method. An operational amplifier was tested by the oscillation-based test strategy, while current monitoring was used to test the resistor ladder. The crucial point of the used test strategy is that the insertion of the necessary additional test hardware might affect the CUT performance. However, with appropriate setting of R_{ON} of the inserted T-gates, this influence can be minimized. T-gates with R_{ON} of about 10 Ω cause area overhead of 13%, and increase of 18% and 27% in INL and DNL parameters, respectively. Catastrophic and parametric faults were considered in the CUT. In the worst case, the total fault coverage of 92.42% and 96% for the OPAMP and the resistor network was achieved, respectively. This is an excellent result especially, if taking into account that the fault coverage up to 94.21% of hard-detectable faults by parametric test of single parts of the DAC has been achieved. The on-chip total fault coverage might be increased by measuring the amplitude of oscillation. However, for evaluation of the amplitude of oscillation, the additional test hardware will be necessary, which would increase the area overhead.

On-chip parametric test of separated parts is a promising strategy to test complex mixed-signal systems. This approach offers the possibility to identify a defective part and makes test of such systems easier or, in some applications, even possible at all. However, it is necessary to maintain the circuit's original functionality and specific parameters. Further research in this field will be focused on realization of BIST structures, based on the oscillation test strategy, which would be generally applicable for digital-to-analog converters as cores used in complex SoCs.

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